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The characteristics of ZnS/Si heterojunction diode fabricated by thermionic vacuum arc

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ABSTRACT

ZnS/p-Si heterojunction diode has been successfully fabricated by depositing the ZnS thin films on p-type Si substrates using thermionic vacuum arc technique (TVA). The structural analysis was performed with X-ray diffraction (XRD) and Atomic force microscopy (AFM). The results revealed that ZnS thin film demonstrates nano-crystalline behavior with very smooth and homogeneous surface properties. The type was determined as n-type and the carrier concentration was found approximately 3.1×10^{17} cm^{-3} of the ZnS thin film by means of Hall Effect measurement. The dark current-voltage (I-V) and the capacitance-voltage (C-V) measurements with different frequencies were performed to determine the characteristics of the ZnS/p-Si heterojunction diode at room temperature. I-V results show that the diode has a good rectifying characteristic with excellent rectification ratio. The electrical parameters of the diode have been obtained by using current transport mechanism. It was found that the barrier height calculated from dark I-V measurements is in good agreement with the value obtained from C-V measurements at a frequency of 1.5 MHz. The series resistance and the built in potential of the fabricated diode were calculated as 3.6 kΩ and 0.7 V using Cheung and Cheung's equation and C-V measurement, respectively. The low cost and effective film production method were utilized to fabrication of heterojunction diode and to investigate characteristics.

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1. Introduction

Semiconductor materials and devices have been extensively studied for years. As a result of these studies, many different semiconductor materials have been developed in the optoelectronic industry such as solar cells, LEDs, lasers diodes, photodiodes, and light dependent resistance (LDR) etc.

Zinc Sulfide (ZnS), one of the IIB-VIA binary group elements, is known as n-type semiconductor compound with direct wide-band gap energy approximately as 3.73 eV at 300 K [1]. Due to this wide-band gap energy, ZnS has high transparency in optical region (visible light and near infrared), high absorption in the ultraviolet region of the electromagnetic spectrum and it plays very important role to use as an antireflective coating for infrared devices and window layers for solar cells [2–4]. Furthermore, ZnS is a piezoelectric and luminescent material with the high refractive index of 2.40 [5]. This feature makes it suitable to develop optoelectronic devices working in UV region such as high efficient tandem solar cells, photodiodes, UV LEDs, and UV laser diodes.

Si-based materials are coated with II-VI group semiconductors to improve electrical properties of the materials. Among this semiconductor groups, the most preferred one is ZnS that it has non-toxic, low cost, high chemical flexibility and good electrical properties. Moreover, the diamond structure of Si and zinc-blend structure of ZnS have very close lattice constants, i.e., 5.431 Å and 5.420 Å, respectively [6] and this feature allows them to form a good heterojunction. A factor that improves the quality of the efficiency in solar cells is lattice parameters, nearly close to each other. Besides, these structural similarities decrease the defects in the interfacial layer.

Up to now various physical and chemical techniques are utilized to grow ZnS thin films onto Si substrates including chemical bath deposition [3], molecular beam epitaxy (MBE) [4], radio-frequency magnetron sputtering [7,8], pulsed laser deposition (PLD) [9], successive ionic layer absorption and reaction (SILAR) [10] and sol-gel spin coating [11].

The heterojunction solar cell properties of the ZnS microdisks deposited onto a p-Si substrate by chemical vapor deposition have reported by Hsiao et al. [3]. Nematollahi et al. [4] investigated

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structural and optical properties of ZnS:Cr/Si film using MBE and PLD techniques and they stated that Cr into ZnS reduces the grain size of the final structures. Huang et al. [7] have fabricated *n*-ZnS/p-Si heterojunction using radio frequency magnetron sputtering. They found that the heterojunction shows a good rectifying behavior. Besides, they investigated the photoresponse of the heterojunction. They showed that ZnS microdisks have the energy band gap of 3.4 eV. The photoluminescence properties of the ZnS/porous Si have investigated by Wang et al. [9]. They used to PLD technique to fabricate heterojunction films. Authors indicated that the growth temperature affects the photoluminescence properties of the heterojunction. Ateş et al. [10] have reported thermal, structural and electrical properties of the Zn/ZnS/n-Si/Au-Sb sandwich structures deposited by using SILAR technique. From current-voltage characteristics, they have calculated ideality factor, barrier height and series resistance as 2.60, 0.71 eV and 3.8 kΩ, respectively at 300 K. Turgut et al. [11] have investigated device performance of Al/ZnS/p-Si/Al heterojunction diode fabricated using the sol-gel technique. They found that the heterojunction diode shows rectification behavior and from electrical measurements, they were calculated some electrical parameters.

However, as mentioned above, the ZnS films were grown on Si substrate by using physical and chemical fabrication techniques in the application has some limitations including, being an expensive method, long production time, low vacuum condition, a choice of a substrate at high temperatures and non-homogeneous surfaces. These restrictions cause some negative effects for production and analysis of the films.

The novelty of this study is to utilize a new method of the fabrication ZnS/Si heterojunction diode and investigate their characteristics. In this context, non-reactive thermionic vacuum arc technique (TVA) has been used [12]. The advantages of this technique are; very short processing time, high deposition rate, very low surface roughness and good adhesion in nanostructured thin films. Furthermore, in the implementation of this technique, a thin film under high vacuum condition can be produced without needed any buffer gas.

2. Experimental details

A p-type Si wafer used in present work has 1–10 Ω cm resistivity and (100) orientation, respectively. Si wafer consecutively was cleaned in ethanol for 5 min, then rinsed deionized pure water, afterward etched in 10% HF acid solution for 2 min and finally, rinsed with deionized pure water in order to remove native oxide layer before making back contact. Al was selected for making ohmic contacts. The back side of Si wafer made ohmic contact (~100 nm) by using thermal evaporation and for good ohmic contact, p-type Si wafer was heat-treated at 400 °C for 10 min in an N_2 atmosphere. After ohmic contact, Si wafer etched in 10% HF acid solution for 2 min to remove the native oxide layer and then rinsed deionized pure water. The surface of the Si wafer was highly hydrophobic after this process. The fabrication process of the ZnS/p-Si heterojunction thermionic vacuum arc technique (TVA) has been used. Detailed information about the working principle of the TVA technique was indicated by Özen et al. [12–14]. We summarized here the working principles of this technique. TVA is composed of an anode and cathode. An anode electrode consists of the crucible and is used for storage of materials while cathode electrode consists of 3 mm diameter tungsten wire surrounded by a Wehnelt cylinder. By using a high dc voltage, accelerated electrons collided with anode using Wehnelt cylinder. Then anode materials begin to melt and evaporate. A stable condition occurs between the anode and the cathode. By increasing the voltage, a bright discharge occurs inside the vacuum chamber due to the evaporation of the anode materials and the coating begins to start.

TVA chamber was evacuated to pressure under the 8×10^{-5} Torr before start to deposition ZnS films. Filament current, acceleration voltage and deposition process time were 18 A, 400 V, and 2 min, respectively. The film thickness of ZnS/p-Si heterojunction has been measured approximately 300 nm by using FilMetrics thin film thickness measurement system. For the front contact, Al was deposited to the other side of Si wafers with thermal evaporation and the thickness and diameter of Al contacts were approximately 100 nm and 2 mm, respectively. Al/n-ZnS/p-Si/Al heterojunction device is obtained by all these processes.

Atomic force microscopy (AFM, NanoMagnetics Instruments) was used to examine the surface morphology of ZnS thin films. The crystalline properties of the ZnS thin films were analyzed by using X-ray diffraction (XRD, Bruker D 8 Advanced), operated at 40 kV, 40 mA and using Cu-Kα radiation (λ = 0.154 nm). To characterize the device parameters of the heterojunction, current-voltage (I-V) (Keithley 6517 electrometer) and capacitance-voltage (C-V) measurements (Hewlett Packard 4192 An LF model impedance analyzer) were performed. The type and the carrier concentration of the ZnS thin film were determined by Hall Effect (HMS 3000 Ecopia).

3. Results and discussion

3.1. Structural and morphological investigation of ZnS/Si heterojunction diode

Fig. 1 depicts XRD spectra of the polycrystalline ZnS thin films grown on p-type Si wafer.

The observed peaks in the film indicated that the thin film corresponds to the cubic structure of polycrystalline ZnS with diffraction planes (111) and (220). (JCPDS card no: 01-072-9262). With this result, it is revealed that there has been a good junction between ZnS thin film and Si substrate. Besides, no impurity or another peak was observed in XRD pattern. The average crystalline size of the ZnS thin film was measured using Debye-Scherrer formula [15] approximately 43 nm for the dominating crystalline

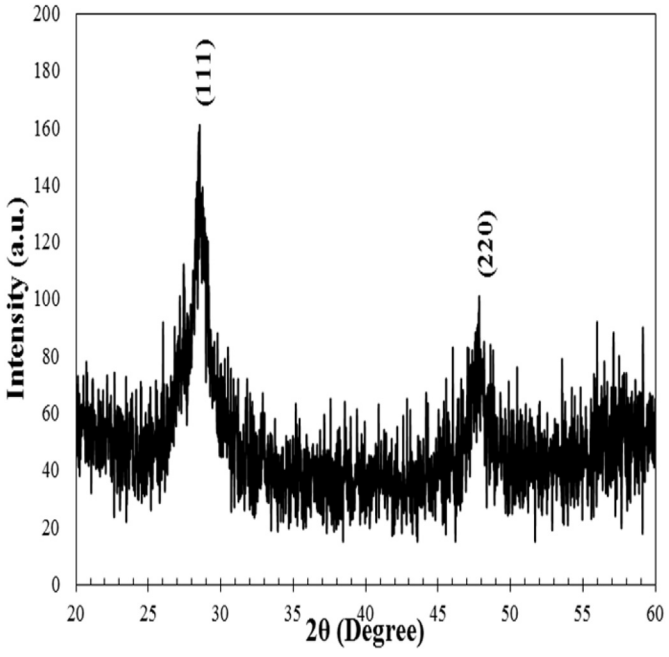


Fig. 1. X-ray diffraction pattern of the ZnS thin film grown on Si substrate.

orientation (111). In addition, by using this dominating orientation, lattice strain and dislocation density [2] were found to be (1.67–8.73) x 10^{-3} and (1.5–5.4) x 10^{14} lines/m^2, respectively.

The surface morphology of the ZnS thin films grown on p-type Si substrate was analyzed by AFM. Fig. 2 shows 2-D and 3-D AFM images of the ZnS thin film surface scanning at 2 × 2 μm^2. As seen in Fig. 2, grains are distributed homogeneously and over the scan area, the root mean square roughness (RMS) of the ZnS/Si heterojunction structure is determined approximately 1.5 nm. This RMS value is very low and compared with Bouguila et al. [1] and Turgut et al. [11] measurements, it is seen that the homogeneous and smoother surface is fabricated using TVA technique. In the literature, there are a few investigation about the surface formation of the ZnS thin film grown by different production methods. Nematollahi et al. [4] have utilized scanning electron microscopy (SEM) to investigate the surface of ZnS thin films. They stated that undoped ZnS films have higher grain size than Cr doped ZnS films. Besides, ZnS films grown by MBE (200 °C substrate temperature) have RMS value of 9.3 nm and the film grown by PLD (500 °C substrate temperature) has RMS value of 2.8 nm. Madugu et al. [5] have used AFM to determine ZnS thin film surface topographies grown on FTO/glass substrates. In the electrodeposition growth method, structural discontinuity and high roughness values have been observed.

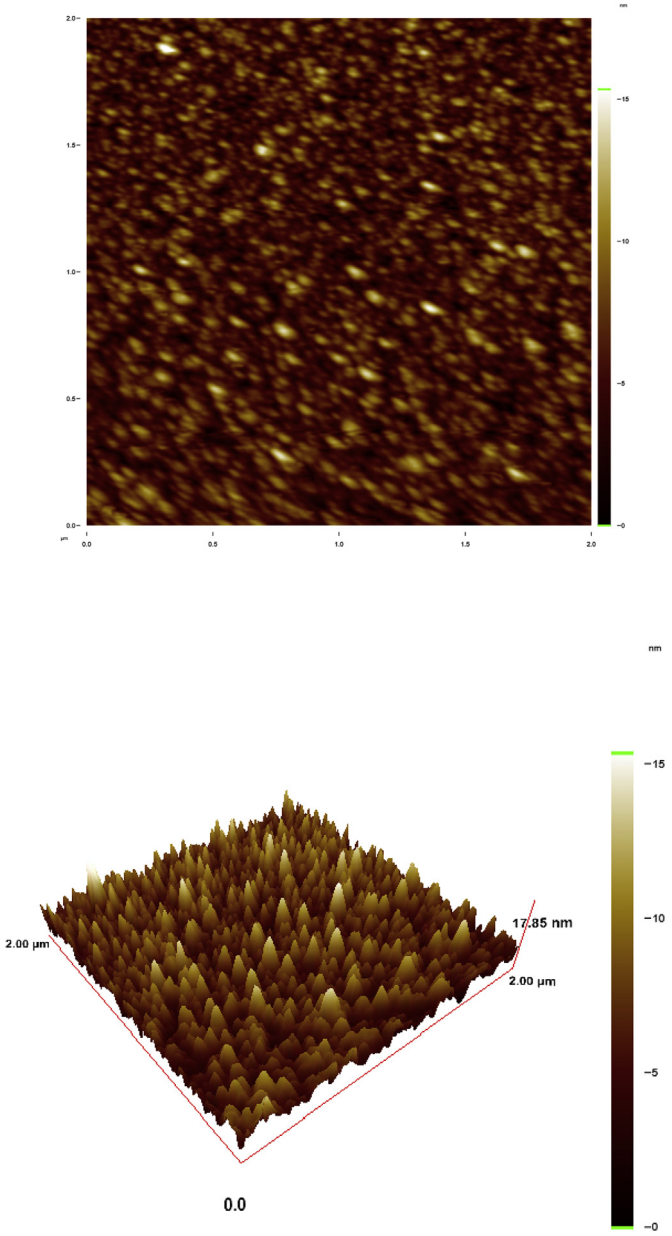


Fig. 2. 2-D and 3-D AFM images (2 × 2μm^2) of the ZnS film surface grown on Si substrate.

3.2. Electrical characterization of ZnS/Si heterojunction diode

In order to determine the electrical parameters of ZnS/Si heterojunction diode, dark I-V measurements were performed at 300 K and are presented in Fig. 3. As seen from the dark I-V plot, the fabricated device shows an excellent rectifying behavior with no leakage current and it indicates p-n heterojunction characteristic. The rectification ratio of our device was calculated as 1100 at ±1.25 V. I-V plot exhibits different behavior in the forward current with bias voltage region (0 < V < 0.55). Semi-logarithmic current versus voltage plot shows that the current increases with the increasing voltage. From the thermionic emission theory known as current transport mechanism used for heterojunction, the current can be written as a function of the applied voltage across the junction as [16]

$$I = I_S\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

Herein, n is the dimensionless parameter called as ideality factor, q is electronic charge, k is the Boltzmann's constant and T is absolute temperature. Saturation current I_S can be expressed as

$$I_S = AA^*T^2\left[\exp\left(\frac{q\phi_b}{kT}\right)\right] \quad (2)$$

Herein, A is diode area, A^* is Richardson constant and ϕ_b is barrier height. An expression can be written for barrier height from Eq. (2) as:

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_S}\right) \quad (3)$$

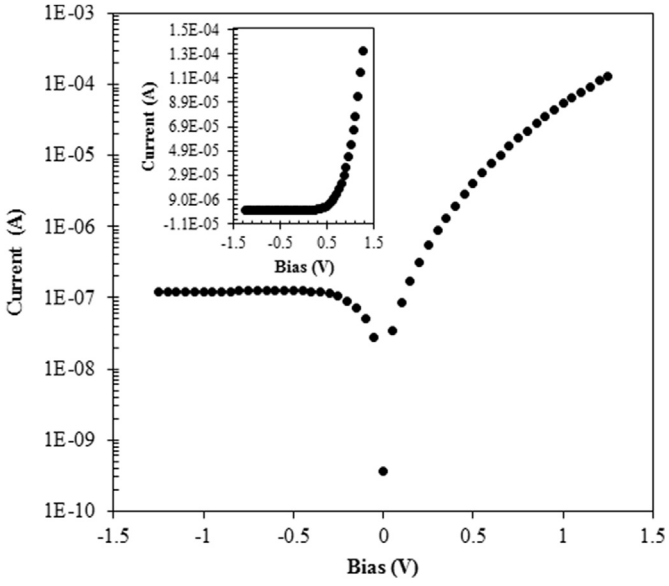


Fig. 3. I-V plots of Al/n-ZnS/p-Si/Al heterojunction device at 300 K. The inset depicts I versus V of Al/n-ZnS/p-Si/Al heterojunction.

Saturation current I_S was obtained by extrapolating semi logarithmic I-V plot to V = 0 and I_S found as approximately 5.36×10^{-8} A. The theoretical value of Richardson constant for p-type Si is $A^* = 32$ A cm^{-2} K^{-2} [17]. By using this saturation current value and Eq. (3), barrier height for the fabricated ZnS/Si heterojunction was calculated as $\phi_b = 0.73 \pm 0.02$ eV.

In addition to this characteristic, ideality factor n derived from Eq. (1) is another parameter and it can be calculated from forward bias I-V plot and defined as [18]

$$n = \frac{q}{kT}\left(\frac{dV}{d(ln(I))}\right) \tag{4}$$

The ideality factor n is found to be 2.72 for low bias voltage region, while for higher bias voltage region, n is found to be 5.21. It is observed that the ideality factor n is increasing with the increasing bias voltage. In this study, n is slightly different from the ideal value of 1 measured at low forward bias and high forward voltage region. This is probably either the interfacial defects or series resistance or might be the existence of an oxide layer between the ZnS thin film and the p-type Si substrate. The ideality factor measured in present work is in good agreement with those reported [7,10,11]. By contrast, the barrier height is found to be better than their results [10,11].

To investigate series resistance effect on the electrical parameters of the ZnS/Si heterojunction diode, Cheung and Cheung's method [19] have been utilized. Nevertheless, Cheung's method also can be used to calculate device parameters.

$$\frac{dV}{d(lnI)} = \frac{nkT}{q} + IR_s \tag{5}$$

Herein, R_S is the series resistance. As can be seen from Fig. 4, experimental dV/d (lnI) versus I plot shows a straight line and using Eq. (5), R_S and n can be determined from the slope of the dV/d (lnI) versus I plot and y axis intercept, respectively.

The n and R_S can be also obtained by Cheung and Cheung's function (H(I)). Experimental H(I) versus I plot shows straight line and the slope of this plot will give series resistance R_S and from the y axis intercept, barrier the height ϕ_b can be calculated by using Eq. (7).

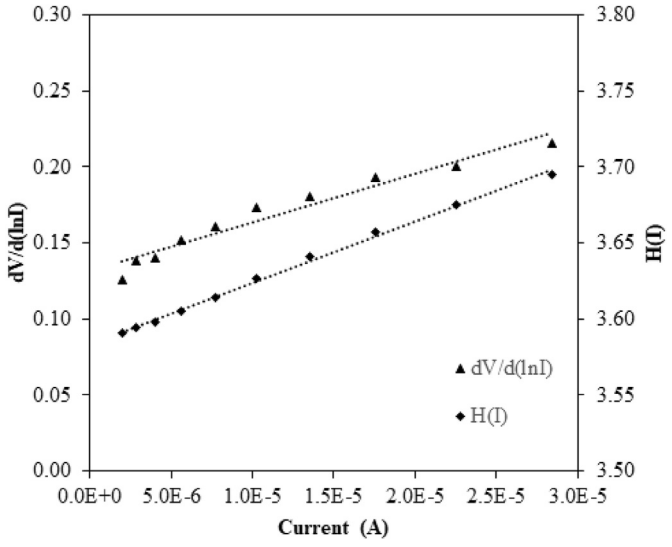


Fig. 4. dV/d (lnI)-I and H(I)-I plots of Al/n-ZnS/p-Si/Al heterojunction device at 300 K.

$$H(I) = V - \left(\frac{nkT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

and

$$H(I) = n\phi_b + IR_s \tag{7}$$

The ideality factor n and series resistance R_S is measured as 5.2 and 3.2 kΩ from experimental dV/d (lnI) versus I plot, while the series resistance and barrier height obtained from H(I) versus I plot is calculated as 4.0 kΩ and 0.70 ± 0.02 eV, respectively. Here, it is seen that the series resistance R_S values obtained using Eqs. (5) and (7) is compatible with each other. The average series resistance R_S of the ZnS/Si heterojunction diode was found to be 3.6 kΩ. The obtained series resistance value here is lower than those reported by Turgut et al. [11]. The I-V results in this work and the related literature data are listed in Table 1.

The room temperature capacitance-voltage (C-V) measurements were fulfilled to determine the interface quality of the junction region and to investigate carrier concentration and barrier height of the heterojunction diode. In the inset of Fig. 5, the forward and reverse bias C-V characteristics of the heterojunction diode at room temperature for different frequencies are shown. It is clearly observed that the capacitance value decreases with increasing frequencies.

In consequence of the donor concentration is quite higher than the acceptor concentration ($N_D \gg N_A$), the junction capacitance per unit area can be described as [20]

$$\frac{A^2}{C^2} = \frac{2\left(V_{bi} - V - \frac{kT}{q}\right)}{\epsilon_S q N_A} \tag{8}$$

Herein, V_{bi}, N_A, and $\in_s$ are built in potential, the carrier concentration and the permittivity of Si ($\varepsilon_s = 11.9\varepsilon_0$), respectively. Other variables have the same meaning as mention before. Fig. 5 shows A^2/C^2 versus V characteristics for all frequencies obtained at room temperature. As seen from Fig. 5, qV_{bi} values were calculated from the point where the linear region intercepts along the x axis and N_A values were calculated from the slope of the plot. These values are listed in Table 2. As seen from Table 2, N_A values are changing from 6.15×10^{15} to 7.23×10^{15} cm^{-3}. This indicates that N_A is in a good conformity with the doping concentration of Si wafer.

The barrier height of the ZnS/Si heterojunction can be measured using C-V plot and can be described as [20]

$$\varnothing_b = V_{bi} + \frac{kT}{q} ln\left(\frac{N_V}{N_A}\right) \tag{9}$$

Herein, N_V is the density of states in valance band. For Si, N_V is equal to 1.0×10^{19} cm^{-3} at 300 K. N_A is the ionized acceptor concentration and all the other variables meaning are mention above. The barrier height values obtained from $A^2/C^2 - V$ plot varied from 1.06 to 0.91 eV by increasing frequency which changing from 50 kHz to 1.5 MHz, respectively. This reduction of the barrier height with increasing frequency of the ac signal indicates that the higher frequencies eliminate the contributions of interfacial defects or an oxide layer at the junction. The barrier height measured at a frequency of 1.5 MHz is in conformity with the barrier height calculated from I-V measurements. The reason of the distinction in barrier height values calculated from C-V and I-V method might be either the interfacial oxide layer or interface state [20]. The calculated results are listed in Table 2.

Table 1
The I-V parameters of ZnS/p-Si heterojunction diode and the related literature data.

	Conventional (I-V) method			Cheung – Cheung's method		
	n	ϕ_b (eV)	I_0 (A)	n	ϕ_b (eV)	R_S
Our work	2.72	0.73	5.36×10^{-8}	5.2	0.69	3.2 kΩ/4.0 kΩ
[7]	1.9	–	–	–	–	–
[10]	2.6 to 1.68	0.71 to 0.62	–	–	–	–
[11]	2.34	0.77	–	4.3	0.77	12.3 kΩ/12.5 kΩ

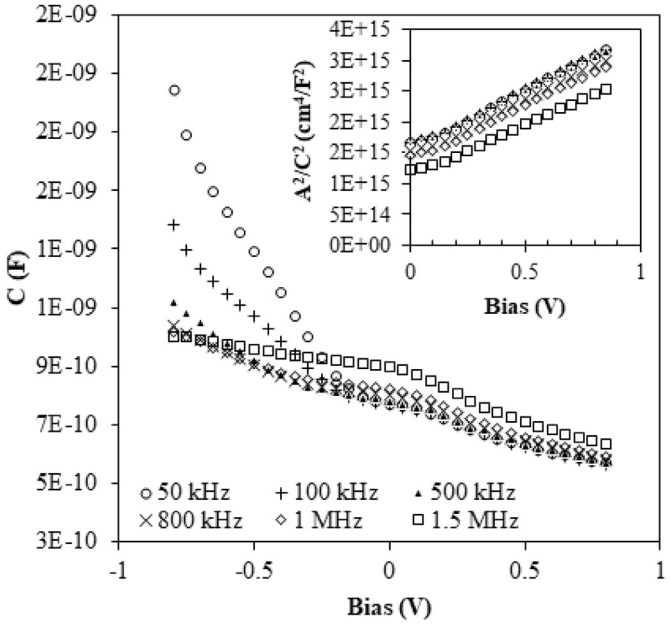


Fig. 5. The reverse bias A^2/C^2-V characteristics of the ZnS/Si heterojunction diode at different frequencies at 300 K. The inset depicts the forward and reverse bias C-V characteristics of the heterojunction diode for different frequencies at room temperature.

Table 2
The C–V analysis results of the ZnS/p-Si heterojunction diode.

Capacitance – Voltage method			
Frequency (kHz)	N_A (cm^{-3})	qV_{bi} (eV)	ϕ_b (eV)
50	6.34×10^{15}	0.84	1.06
100	6.28×10^{15}	0.82	1.04
500	6.15×10^{15}	0.77	0.99
800	6.48×10^{15}	0.79	1.01
1000	6.59×10^{15}	0.76	0.98
1500	7.23×10^{15}	0.70	0.91

4. Conclusion

ZnS/Si heterojunction device was successfully fabricated by using thermionic vacuum arc technique. The characterization of ZnS film and the parameters of the ZnS/Si heterojunction diode were determined in detailed. XRD results demonstrate that the produced ZnS thin film has a cubic crystal structure. AFM image revealed the homogeneous distribution of the ZnS thin film on Si substrate with 1 nm surface roughness. The carrier concentration and the type of the ZnS thin film were obtained as 3.1×10^{17} cm^{-3} and n-type at the room temperature. ZnS/Si heterojunction diode shows an excellent rectifying behavior at room temperature. The main electrical parameters for heterojunction diode are investigated. The ideality factor and the zero bias barrier height of the heterojunction diode are determined by using I-V and C-V measurements. The barrier height value is found in good agreement with both the dark I-V and at a frequency of 1.5 MHz C-V measurements at 300 K. Series resistance value was measured by using Cheung and Cheung's formulas as 3.6 kΩ and 4.0 kΩ. Fabricated device demonstrate p-n characteristics in dark at 300 K. Results indicate that TVA technique can be an important production method for fabricate thin films with excellent electrical properties in a short period of time such as 2 min. With this context, it can be said that according to other production methods and techniques, TVA technique has a significant advantage in production for thin films due to its low cost and short production time. In a subsequent study, optoelectronic properties of the ZnS/p-Si heterojunction diode will investigate.

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